

DAY 1:

INTEL DSP BUILDER HIGH-LEVEL SYNTHESIS

SESSION TOPICS

- INTRODUCTION TO DSP BUILDER FOR INTEL FPGAS, INTERFACE BETWEEN MATLAB, AND SIMULINK TOOLS
- INCORPORATING A DSP BUILDER MODEL INTO A SYSTEM, HARDWARE PERFORMANCE AND IMPLEMENTATION- DEMO
- INTRODUCTION TO HLS COMPILER, X86 EMULATION AND CO-SIMULATION, INTEL QUARTUS INTEGRATION AND SYSTEM INTEGRATION
- HLS IMPLEMENTATION OF A 32-BIT SQUARE ROOT COMPONENT - DEMO

DAY 2:

CONVERSATIONAL AI NLP and FPGA FPGA ACCELERATION HIGH-SPEED INTERFACES

SESSION TOPICS

- FPGAS AND MACHINE LEARNING, CONVERSATIONAL AI, NLP AND FPGA, ACCELERATING AI WITH INTEL STRATIX 10 NX FPGA
- INTRODUCTION TO FPGA ACCELERATION AND ACCELERATION STACK OVERVIEW,COMPILING THE AFU INTO AN ACCELERATOR FUNCTION,FPGA DEVCLOUD
- INTRODUCTION TO HIGH SPEED I/O, SERIALIZER AND DESERIALIZER,CHALLENGES IN HIGH SPEED I/O
- CYCLONE V TRANSCEIVER DESIGN FLOW, SIMULATION AND DEMONSTRATION

Resource Persons:

Mr.Padmanaban K
Program Specialist – India FPGA
University Outreach
Intel Programmable Solutions
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Intel India

&

Mr.Ritesh Belgudri
Field Applications Engineer
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Online FDP

on

**DSP Builder, AI,
FPGA Accelerator using
Intel FPGA**

Important Dates

Last Date for Registration: 23/06/21

25/06/2021

&

26/06/2021

TIMINGS

9:00 AM TO 1:00 PM

Registration Link:

<https://forms.gle/1PvTAThkCcHsa8ZC9>

Coordinators

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Organized by

**School of Electronics
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