



VIT[®]
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Volume 1 Issue 1
December 2023

Centre for nanoelectronics and VLSI design
VIT Chennai

C NVD Chronicles



- About CNVD
- Vision & Mission
- Activities
- Publications
- Funded Projects
- Patents
- Faculty visit abroad
- Glimpse of events

About CNVD

The modern electronic systems are prevalent as an essential and integral part of human life in terms of industrial and consumer electronics products. A few notable subsystems are processors, controllers, multimedia equipment and networking modules. Integration of such subsystems forms macro systems to cater for various promising applications resulting in revolution of infotainment systems, wireless communication equipment, analog/digital signal processors, medical instruments. Miniaturized product development is made feasible through the advancements in IC design, microsensors and modern nano-devices. The Centre for Nano-electronics and VLSI design (CNVD) is established in January 2020 with the motivation to excel in the state-of-the-art CMOS Integrated Circuit design that will pave way in the research and development of electronic system design, specifically in domain such as Digital VLSI Design, Analog & Mixed Signal IC design, Nano-electronic devices and FPGA based system designs. CNVD will also promote high quality education in VLSI Design and Embedded Systems that will lead to product development and commercialization. The focus areas of the centre are

- Modeling and Simulations of Nano-electronic Devices and Circuits
- MEMS device design and integration of CMOS electronics
- Digital and Analog VLSI Design
- FPGA based System Design

Vision

To become an internationally renowned centre in the area of Nano-electronics and VLSI design through high quality research and innovations that cater to the development of our country.

Mission

- To pursue innovative and cutting-edge research in nano-scaled devices, analog and digital IC design, MEMS and FPGA based systems for industrial and consumer electronics applications.
- To advance in electronic product development which provides effective solutions for societal and industrial needs.
- To train engineers and researchers in the field of nano-electronics and VLSI design.

Activities

Events Organized

Topic of the event	Name & Affiliation of Speakers	Coordinators	Date of Talk
MEMS Design to Realization	Dr Sripadaraja. K, Managing Partner, Intellisense, Bangalore, India	Dr. Ananiah Durai S Dr. Manikandan. P	27 th March 2023
Abstraction Levels of Computer Design	Engineer II ASIC Design, Open Five Technologies, BLR	Dr. A. Anita Angeline Dr. Prathiba A	6 th April 2023
Hardware accelerator and solution design concept using SOC-FPGA	Mr. Prasanna Venkatesh Balasubramaniyan, Group Technical Manager HCL Technologies Chennai	Dr. A. Anita Angeline Dr. Sasipriya P	4 th April 2023
Digitization in Industries	Dr. R. Vijayarajeswaran Managing Director VI microsystems	Dr. Gargi Raina Dr. Prathiba	22 nd May 2023
Opportunities and Challenges in FPGA Design	Mr. Padmanaban K Program Specialist –India FPGA University Outreach Intel Programmable Solutions Group, Intel, India	Dr. A Prathiba Dr. P Augusta Sophy Beulet Dr. A. Anita Angeline	2 nd August 2023
Focus on VLSI Physical Design	Ms. Monica Padmanabhan SOC Design Engineer, Intel Corporation, Folsom California, United States	Dr. Umadevi S Dr. Ravi Sankar A	18 th October 2022
Digital IC design using Cadence Virtuoso	Dr. Anita Angeline A, Associate Professor (Sr), SENSE Dr. Sasipriya. P, Associate Professor(Sr), SENSE	Dr. Sasipriya. P Dr. A. Anita Angeline	10 th & 11 th Oct 2022
Workshop on VLSI Design	Dr. Anita Angeline A, Associate Professor (Sr), SENSE Dr. Sasipriya. P, Associate Professor(Sr), SENSE	Dr. Sasipriya.P Dr. A. Anita Angeline	19 th & 20 th Sep. 2023
Workshop on physical design and verification	Dr. Umadevi S Dr. Sakthivel S M	Dr. Umadevi S Dr. Sakthivel S M	23 rd Sep. 2023

Guest Lecture on Embedded Systems-an industry perspective	Mr. Jeyaraman, Enphase Energy, Bangalore	Dr. G. Gugapriya Dr. B. Lakshmi	3 rd Nov. 2023
Workshop on Digital IC design using Cadence Virtuoso	Dr. Anita Angeline A, Associate Professor (Sr), SENSE Dr. Sasipriya. P, Associate Professor (Sr), SENSE	Dr. Sasipriya. P Dr. A. Anita Angeline	10 th & 11 th Oct. 2023
Workshop on VLSI Design	Dr. Anita Angeline A, Associate Professor (Sr), SENSE Dr. Sasipriya. P, Associate Professor(Sr), SENSE	Dr. Anita Angeline. A Dr. Sasipriya. P	19 th & 20 th Sep. 2023

Invited Talks

Title of the Talk	Speaker	Name of the Institution/Industry	Date of Talk
Talk on Integration techniques of CMOS-MEMS Design	Dr Ananiah Durai	Intellisuite Ltd. Bangalore	20 th July 2023

Publications

- M. M. Sravani and S. A. Durai, "Bio-Hash Secured Hardware e-Health Record System," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 17, no. 3, pp. 420-432, June 2023, doi: 10.1109/TBCAS.2023.3263177.
- Lokesh Boggarapu and B Lakshmi, "Implementation and performance analysis of QPSK system using pocket double gate asymmetric JLTFET for satellite communications", *Scientific Reports*, Vol.13, No.1, February 2023.
- K Aishwarya and B Lakshmi, "Investigation of heavy ion radiation and temperature on junctionless tunnel field effect transistor", *Journal of nanoparticle Research*, Vol.25, No.7, June 2023.
- Kalavathi Devi, T., Baluprithviraj, K. N., Madhan Mohan, M., Uma Devi, S., Sakthivel, P., Rajeshwari, P., and Vinodha, B, "Non-invasive method for the prediction of micronutrient deficiency using sequential learning techniques", *Computer Methods in Biomechanics and Biomedical Engineering: Imaging & Visualization*, Vol 11, June 2023.
- S Pavani., Augusta Sophy Beulet P., "Improved Precision Crop Yield Prediction Using Weighted-Feature Hybrid SVM: Analysis of ML Algorithms", *IETE Journal of Research*, DOI: 10.1080/03772063.2023.2192000 (IF: 1.877).
- Kulkarni A., Beulet P.A.S., "Sensor-based adaptive estimation in a hybrid environment employing state estimator filters, *Intelligent Automation and Soft Computing*", Vol:37, Issue: 1, Pg.No(127-146), DOI: 10.32604/iasc.2023.035144 (IF:3.407).
- Lee Mun Feng, Nabihah @ Nornabihah binti Ahmad, Chessda Uttraphan A/I Eh Kan, Ananiah Durai. S, Warsuzarina Mat Jubadi presented the paper entitled "ASIC-Based Facial Emotion Recognition System For Human-Computer Interaction" in *International Conference on Electrical & Electronic Engineering 2023 (Icon3E2023)*, 28th & 29th August 2023
- Julee Choudhary, Ananiah Durai. S, Nabihah @ Nornabihah binti Ahmad presented a paper entitled, "Smart Microfluidic Devices For Point-Of-Care Applications", in *International Conference on Electrical & Electronic Engineering 2023 (Icon3E2023)*, 28th & 29th August 2023.
- R. Raiashree, S. A. Durai, M. S. Murali, P. Manideep and M. R. Kannan, "Elliptic Curve Scalar Multiplication over Prime Field for both Affine and Jacobian Coordinates," *2023 International Conference on Intelligent and Innovative Technologies in Computing, Electrical and Electronics (IITCEE)*, Bengaluru, India, 2023, pp. 232-237, doi: 10.1109/IITCEE57236.2023.10090927.
- Kalavathidevi T, Umadevi S, Ramesh S, Renukadevi D and Revathi S," IoT-based color fault detection using TCS3200 in textile industry", *Integrated Green Energy Solutions*, 2023, 1, pp. 309–326, Wiley publication.
- Benjamin and B. Bindu, "Analysis of single event transients and voltage perturbations in GaN based C-FinFET inverter", *XXII International Workshop on Physics of Semiconductor Devices (IWPSD)*, 2023
- Y. M. Aneesh & B. Bindu, "Comparative Analysis of Single Event Transients in InGaAs-OI/Bulk/ BOI FinFETs for SET-Tolerant InGaAs/Ge-OI Complementary FinFET Circuits", *IETE Journal of Research*, May 2023 (DOI: 10.1080/03772063.2023.2204836).

Funded Projects

Principal Investigators	Name of the Agency	Title of the Project	Total Amount (in Lacs)	Period of support	Completed/ Ongoing
Dr Ananiah Durai. S	VIT Seed Fund	Design and development of hybrid crypto system for secured access of health record	3.05	January 2023 to January 2025	Ongoing
PI: Dr Nabihah Ahmad, UTHM University. Co-PI: Dr Ananiah Durai. S	FRGS Grant - Ministry of Higher Education, Malaysia	Duplex AESHA3 Lightweight Crypto-Hardware for Medical IOT Device security with new SubBytes architecture	18	01/09/2022 till 31/08/2025	Ongoing
Dr. B. Bindu	VIT-International Research Fund Scheme (VIN) award	To visit University of Glasgow, UK for collaborative research for a period of 3 months	3	September to October 2023	Ongoing
Dr P Sasipirya & Dr A Anita Angeline	DST-SERB	National Seminar on “VLSI Design – Trends and Practices”	2	3 days	Completed
Dr. Ananiah Durai	Consultancy project: CIIRC, Jyothy Institute of Technology, Tataguni, Bangalore	Design and Implementation of interface Electronic Circuitry for Bio – MEMS Sensor	2	2022-2023	Completed
Dr A Prathiba Dr P Augusta Sophy Beulet Dr M Sivagami	VIT SEED FUND	Design and Development of masked PRESENT lightweight block cipher soft IP core	3.6	FY 22-23	Ongoing
Dr. Sasipriya. P & Dr. Anita Angeline A	Consultancy project: Zerlin Energy, Chennai	Debugging of Alektra coding for ICs and study of solid state relay's (SSR)	0.2	2023-2024	ongoing

Patents filed

Patent Title: DEVICE FOR ENABLING UNDERWATER DATA COMMUNICATION BY USING JUNCTIONLESS TUNNELFET (JLTFET)

Investigators: B Lakshmi & B Lokesh

Filed Date: Nov 27, 2023

File No: 202341080254

Faculty visit abroad

Research Visit University of Glasgow, Semiwise and Synopsis, Glasgow, UK - October 1st to November 1st, 2023 with financial support through VIT – Foreign University Research Fund Scheme for the year 2022-23

I. Invited Talk on 16th October 2023



II. MoU signed with Semiwise, spin-off company of Glasgow University for research collaboration



III. Visit to Synopsis, Glasgow, UK



IV. Research Visit to Nagasaki, Tokyo and Yokohama National University, Japan

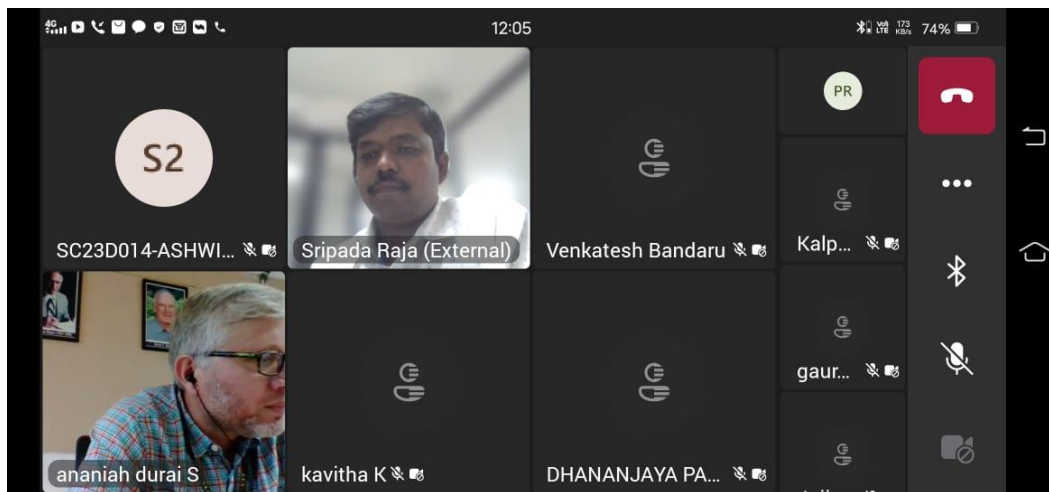


Glimpse of events

Invited Talk

An invited Talk on CMOS+MEMS Design Techniques on 20/07/2023 to the industry, Intellisuite Ltd. Bangalore has been delivered by DR. Ananiah Durai. The Highlights of the talk are design techniques of multistage sensor readout were discussed. The signal pick up and conditioning include the following;

- The weak noisy input current is initially converted into a voltage
- Voltage signal is then amplified using a low-noise high gain chopper-stabilized folded cascade opamp.
- The high frequency chopper residuals are filtered out by a higher-order steep roll-off Gm-C low-pass filter.
- output buffer at the final stage should be capable of driving a large off-chip load of up to 15 pF




Workshop at Technovit


A *Cybersecurity* Workshop has been organized on 13th September 2022 as a part of Technovit'2022 and Mr.Sibidharan Nandhakumar, CEO and Managing Director, Selfmade Ninja Academy, Bangalore introduced to the students on the following topics.

- Introduction to Cybersecurity
- Social Engineering
- Explanation of Cyberattacks
- DDOS
- QA


The event is open to students in all branch of Engineering and was organized by the coordinators, Dr.A.Anita Angeline & Dr. A Prathiba of CNVD




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INSTITUTION'S INNOVATION COUNCIL
Division of IIC Cell




Environmental Sustainability

CYBER SECURITY WORKSHOP



WITH
Mr. Sibidharan Nandhakumar
CEO, CHIEF INSTRUCTOR : SELFMADE NINJA ACADEMY




HIGHLIGHTS

- LIVE DEMONSTRATION OF CYBER ATTACKS
- BEHIND THE SCENES OF CYBER ATTACKS
- HOW TO GET STARTED IN CYBER SECURITY
- Q/A

REGISTRATION FEE: Rs.100

DATE: 13.09.2022
TIME: 6:00 PM - 7:30 PM
VENUE : ZOOM MEETING

SCAN TO REGISTER



<p>Faculty Co-ordinator Dr Anita Angeline A 9500006792 Dr.Prathiba A 8144415162</p>	<p>Student Co-ordinator Jeeva Pranesh 8675737202 Aisurya Mishra 6360948727</p>
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Advisory Board

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