REGISTRATION LINK:

https://forms.gle/cHDQjGmRwSUTnCXV9

DATES TO REMEMBER

Last date for applying : 10th Sep 2021

Confirmation to the participants : 13th Sep 2021

*E-Certificate will be provided

ADDRESS FOR COMMUNICATION

Dr.Sasipriya.P
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ONLINE MEETING

Participants are requested to attend the online sessions and discussion over ZOOM. The detailed schedule and meeting links will be sent to individual participants by an email after the completion of registration.

VIT CHENNAI

VIT for the past 36 years has made amark in the field of higher education in India imparting quality education in a multicultural ambience, intertwined with extensive application-oriented research. VIT was established with the aim to provide quality higher education on par with International Standards. It persistently seeks and adopts innovative methods to improve the quality of higher education on a consistent basis. VIT was established by a well-known educationalist and former parliamentarian, Dr. G. Viswanathan, Founder and Chancellor, a visionary who transformed VIT into a center of excellence in higher technical education. Govt. of India recognized VIT as an Institution of Eminence (IoE). ARIIA, Govt. of India recognized VIT as a No. 1 Private University for Innovation. MHRD, Govt. of India ranked VIT as No.15 among the Engineering Institutions (NIRF-2020 ranking). VIT Chennai is ably spearheaded by Mr. Sankar Viswanathan, Vice President, Ms. Kadhambari S Viswanathan, Assistant Vice President, Dr. Rambabu Kodali, Vice-Chancellor and Dr. V. S. Kanchana Bhaaskaran, Pro- Vice-Chancellor. They share in the mission to make VIT a global center. The focus is:

- To maximize the industrial connectivity
- To create Centers of Excellence in contemporary areas of research
- To enrich technological and managerial human capital nurtured in a multicultural ambience
- To provide a common platform for the agglomeration of ideas of personnel from various walks of life for learning enrichment
- To create opportunities and exploit the available resources to benefit industry/society
- To encourage participation in the National Agenda of knowledge building
- To foster international collaborations for mutual benefits in areas of research
- To maximize the Industrial connectivity
- To create Centers of Excellence in contemporary areas of research
- To enrich Technological and Managerial Human Capital nurtured in a multicultural ambience

VIT – A Place to learn; A Chance to grow
VIT – Recognised as an Institute of Eminence (IoE)

VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Presents

Online Faculty Development Program on

Trends in SoC Design

15th to 17th September, 2021

Organised by

Centre for Nanoelectronics and VLSI Design

Coordinators

Dr.Sasipriya.P
Dr. Anita Angeline A
Centre for Nanoelectronics and VLSI Design
VIT Chennai

ABOUT CNVD

The Centre for Nanoelectronics and VLSI Design (CNVD) was established in March 2020. The centre mainly focuses on the design, modeling and fabrication of nano-scaled devices and integrated circuits for the industrial and consumer electronics applications. The major research areas of the centre are:

- Low power digital VLSI circuits
- Analog integrated circuits
- MEMS and CMOS integration
- Nanoscale devices and circuits
- Hardware security
- FPGA based systems

ABOUT THE PROGRAM

The Vellore Institute of Technology, Chennai is organizing an Online Faculty Development Program on **Trends in SoC Design** from 15*th Sep to 17th Sep 2021*. The main objective of this program is to provide the concepts and challenges in SoC Design. It provides an insight into SoC design, from specification to validation. The niche challenges in the design process are addressed from the circuit design perspective. Further, it extends to the interface protocols and intellectual property of the SoC designs. It also embarks on the design methodology of hardware acceleration for AI processor towards edge applications.

SCHEDULE:

15th Sep 8.30 am	**Accelerator development for ML workloads** *Prerana Maslekar* *AI Hardware Engineer, Microsoft,* *UT- Austin, USA*
10 30 am	**Low Power Chips - Architecture to Silicon Spectrum** Dr Arun Janarthanan, *Low Power Architect, Intel Corporation, Sr. Staff, Qualcomm* *Chennai, India*
16th Sep 9:30 am	**Low Power Circuit Design** *Dr V S Kanchana Bhaaskaran,* *Professor & Pro-VC, VIT Chennai, India*
2 pm	**Low Power Wireless Connectivity** *Meshach Davaraj* *Senior Principal Architect,* *Dialog Semiconductor, UK*
17th Sep 8:30 am	**FPGA based Prototyping** *Dr.Selvakumar Ramasethu,* *Senior Principal Engineer,* *Cadence Design Systems, SJ, USA*
11 am	**Digital Design Process** *Theiventhiran.M* *Digital Design Engineer Staff,* *Synopsys India Pvt. Ltd., Bangalore*

RESOURCE PERSONS:

Ms.Prerana *is an young energetic person. Her expertise includes AI/ML Accelerator Design, Performance Analysis, Design of computer architecture primarily microprocessor architecture, memory management and security.*

Dr.Arun *enjoys the Silicon spectrum from device physics to HW-SW architectures, power and performance of SoCs and has been in various capacities with Qualcomm, Chennai. Previously worked in Intel, Santa Clara and Bangalore.*

Dr.Kanchana Bhaaskaran *has nearly 40 years of industrial, teaching and research experience. Her areas of specialization include VLSI Design for Low Power, Microprocessor Architectures and Linear Integrated Circuits.*

Mr.Meshach Davaraj *has been developing software for short-range wireless communication protocols on various embedded platforms and architecting them. He is an expert in Bluetooth with 21 years of experience.*

Dr.Selvakumar *has 16+ Years of experience in the field of FPGA design, product development, validation, management of FPGA based prototyping and emulation.*

Mr. Theiventhiran *has 16+ years of experience in Semiconductor industry out of which 4 Years in California, USA (Silicon Valley). He has rich experience in frontend RTL design and defined many architecture specifications for memory controller Projects.*

CNVD, VIT Chennai