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VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Centre for Nanoelectronics and VLSI design
VIT Chennai

CNVD Chronicles

About CNVD

The modern electronic systems are prevalent as an essential and integral part of human life in terms of industrial and consumer electronics products. A few notable subsystems are processors, controllers, multimedia equipment and networking modules. Integration of such subsystems forms macro systems to cater for various promising applications resulting in revolution of infotainment systems, wireless communication equipment, analog/digital signal processors, medical instruments. Miniaturized product development is made feasible through the advancements in IC design, microsensors and modern nano-devices. The Centre for Nano-electronics and VLSI design (CNVD) is established in January 2020 with the motivation to excel in the state-of-the-art CMOS Integrated Circuit design that will pave way in the research and development of electronic system design, specifically in domain such as Digital VLSI Design, Analog & Mixed Signal IC design, Nano-electronic devices and FPGA based system designs. CNVD will also promote high quality education in VLSI Design and Embedded Systems that will lead to product development and commercialization. The focus areas of the centre are

- Modeling and Simulations of Nano-electronic Devices and Circuits
- MEMS device design and integration of CMOS electronics
- Digital and Analog VLSI Design
- FPGA based System Design

Vision

To become an internationally renowned centre in the area of Nano-electronics and VLSI design through high quality research and innovations that cater to the development of our country.

Mission

- To pursue innovative and cutting-edge research in nano-scaled devices, analog and digital IC design, MEMS and FPGA based systems for industrial and consumer electronics applications.
- To advance in electronic product development which provides effective solutions for societal and industrial needs.
- To train engineers and researchers in the field of nano-electronics and VLSI design.

Activities

Events Organized

Topic	Name & Affiliation of Speaker	Co-ordinators	Date of Talk
Photonic IC and Microelectronics Design	Dr Sripadraja. K IntelliSense Software, Bangalore & Dr Jaspreet Singh Founder, Fiberonics VPI Photonics	Dr Ananiah Durai. S Dr Sangeetha. R. G	16-04-2024 & 18-04-2024
Electronics in Power Grid	Tarlochan Sidhu Professor at Ontario Tech University Ontario Tech University Oshawa, Ontario, Canada	Dr Ananiah Durai	21-02-2024
Power Optimization Techniques	Mr Vishal Gudavarappu CPU Engineer at Qualcomm Texas, USA	Dr.A.Anita Angeline Dr.Sasipriya P	16-03-2024
An overview of device, circuit and systems	Mr. Lokesh B DFT Design Engineer Intel Bangalore	Dr. B Lakshmi	28-02-2024
FPGA & ASIC Approaches for Advanced Digital System Design	1. Dr.P.Reena Monica Professor. SENSE 2. Dr A Anita Angeline Asso Professor, CNVD 3. Dr P Sasipriya Asso Professor, CNVD 4. Dr P Augusta Sophy Professor. SENSE 5. Dr Prathiba A	Dr. P Augusta Sophy Beulet Dr.Sasipriya.P Dr.A.Anita Angeline	03-06-2024 to 07-06-2024
An overview of RISC V Processor	Mr.Haridhra Kajan Rajkumar, ASIC Digital Design Engineer I, Synopsys	Dr.A.Anita Angeline Dr. Prathiba A	27-02-2024
RISC-V: Exploring the Open-Source	Mr.Enoch Richbert Jebakumar &	Dr. P Augusta Sophy Beulet Dr. Prathiba A	28-02-2024

Architecture Revolutionizing Computing	Mr. Sai Manohar Microchip Technologies,Chennai		
Advancements in VLSI Testing	**Mr. V. Suresh Kumar** Scan Architect/Methodology, Ampere Computing India Pvt. Ltd **Mr. Deepu Alex** Scan Architect/CAD automation Ampere Computing India Pvt. Ltd **Mrs. Renu Nashier** Scan, MBIST, JTAG expert Ampere Computing India Pvt. Ltd.	Dr. S. Umadevi Dr. E. Papanasam	23-03-2024
VLSI Testing and Testability	Mr.Nitesh Mishra Digital Design Manager, Texas Instruments Bangalore	Dr. S. Umadevi Dr. E. Papanasam	27-03-2024

Publications

- A AER, Ahmad NB, S AD. Breast cancer diagnosis through an optimization-driven multispectral gamma correction (ODMGC). Int J Adapt Control Signal Process. 2024; 38(6): 2178-2199. doi: 10.1002/acs.3798
- Kiran Kolluri, S.S., Ananiah Durai, S.: Wearable micro-electro-mechanical systems pressure sensors in health care: advancements and trends—A review. IET Wirel. Sens. Syst. 1–15 (2024). https://doi.org/10.1049/wss2.12084
- Choudhary B.K.J., Durai S.A., Ahmad N.,Journal of Advanced Research in Fluid Mechanics and Thermal Sciences, Vol:114, Issue: 1, Pg.No(119-133), DOI: 10.37934/arfmts.114.1.119133 (31-03-2024)
- Vishal Gundavarapu, P. Gowtham, A. Anita Angeline, P. Sasipriya, Design and evaluation of low power and area efficient approximate Booth multipliers for error tolerant applications, Microprocessors and Microsystems, Volume 106, 2024, 105036, ISSN 0141-9331,

- Rajashree, R. & Durai, S, “FPGA Implementation of DNA Computing and Genetic Algorithm Based Image Encryption Technique, pp. 418-432, March 2024
- Aishwarya, K., and B. Lakshmi. "TCAD simulation study of heavy ion radiation effects on hetero junctionless tunnel field effect transistor." *Scientific Reports* 14, no. 1 (2024): 7643.
- Aneesh, Y. M., B. Bindu, and Asen Asenov. "Single Event Transient Effects in Raised Source/Drain Double-Gate 1-T DRAM." In *2024 8th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, pp. 1-3. IEEE, 2024.
- Nivetha, T., and B. Bindu. "Variability in Switching Characteristics of RRAM Based 1T-1R Configuration and Memory Array." In *2024 IEEE 4th International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA)*, pp. 1-5. IEEE, 2024.
- Banu, Anjana Jyothi, A. Prathiba, S. Shyam Krishna, Suraj Peddhibhotla, and V. S. Kanchana Bhaaskaran. "Profiled Side Channel Power Attack on Charge Balancing Symmetric Pre-Resolve Adiabatic Logic PRESENT S-Box Using Convolutional Neural Networks." *Smart Grids as Cyber Physical Systems: Smart Grids Paving the Way to Smart Cities* 2 (2024): 245-275.
- Natarajan, Kailash, R. Sricharan, M. Thriambak, Anjana Jyothi Banu, A. Prathiba, and V. S. Kanchana Bhaaskaran. "Power Attack Vulnerability Assessment of Circuit-Level PRESENT Encryption IP Using Artificial Intelligence Mechanisms." *Journal of Circuits, Systems and Computers* (2024): 2450245.
- Banu, Anjana Jyothi, Sai Nikhil Varada, V. Yashwanth Raj, S. Sangavi, S. S. Sriram, Aayush Karthikeyan, A. Prathiba, and VS Kanchana Bhaaskaran. "Machine learning based side channel power attack analysis of VLSI implementations in microgrids." In *Next-Generation Cyber-Physical Microgrid Systems*, pp. 185-213. Elsevier, 2024.
- KalavathiDevi, T., K. S. Renuka Devi, S. Umadevi, P. Sakthivel, and Seokbum Ko. "Low power adders using asynchronous pipelined modified low voltage MCML for signal processing and communication applications." *Analog Integrated Circuits and Signal Processing* 118, no. 2 (2024): 343-353.
- Kalavathi Devi, T., S. Umadevi, P. Sakthivel, and K. S. Renuha Devi. "IoT-Based Optimal Power Generation Monitoring in Hybrid Power Plant System for Effective Grid Maintenance." *Smart Grids as Cyber Physical Systems: Smart Grids Paving the Way to Smart Cities* 2 (2024): 229-243.

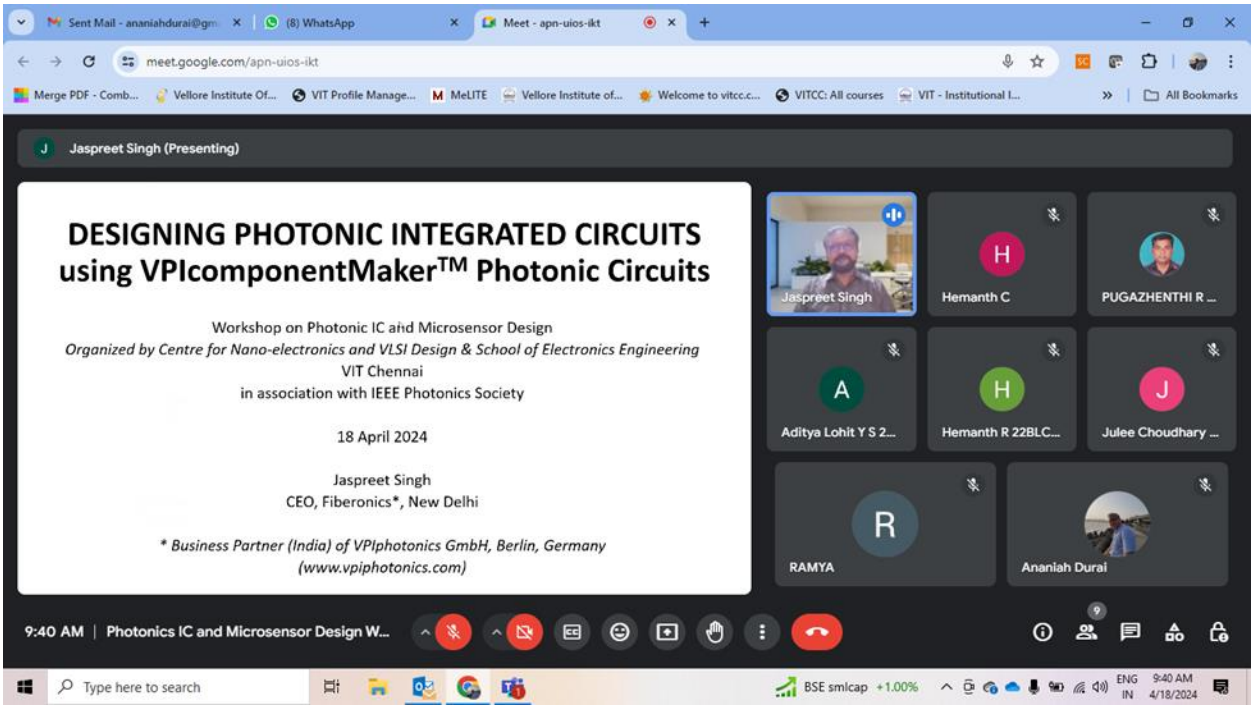
Patents

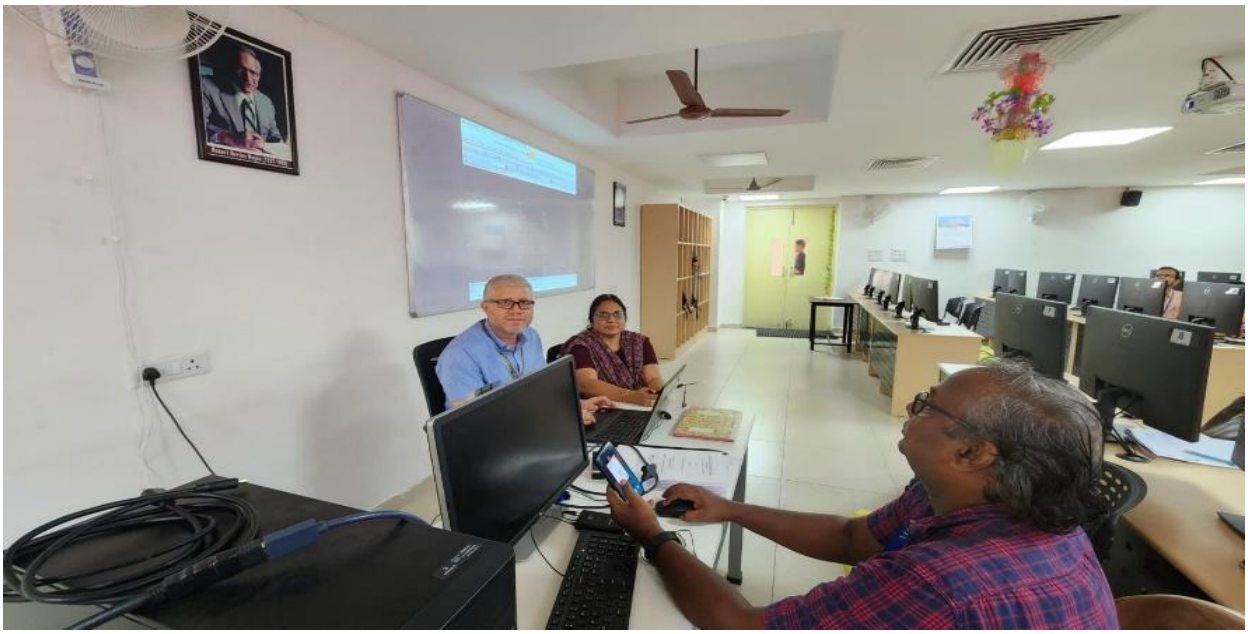
- Gowtham Pandiarajan, Sasipriya P & Anita Angeline A, APPROXIMATE RESTORING LOG DIVIDERS WITH HIGH PERFORMANCE, Published on 21.6.2024 App No: 202441044041
- S Umadevi, Sruthi Venkatesh, Prathiba A, SYSTEM AND METHOD FOR ENABLING TIMING CLOSURE IN SYSTEM-ON-CHIP (SOC) Published on 09-02-2024 App No: 202441001929

Funded Projects

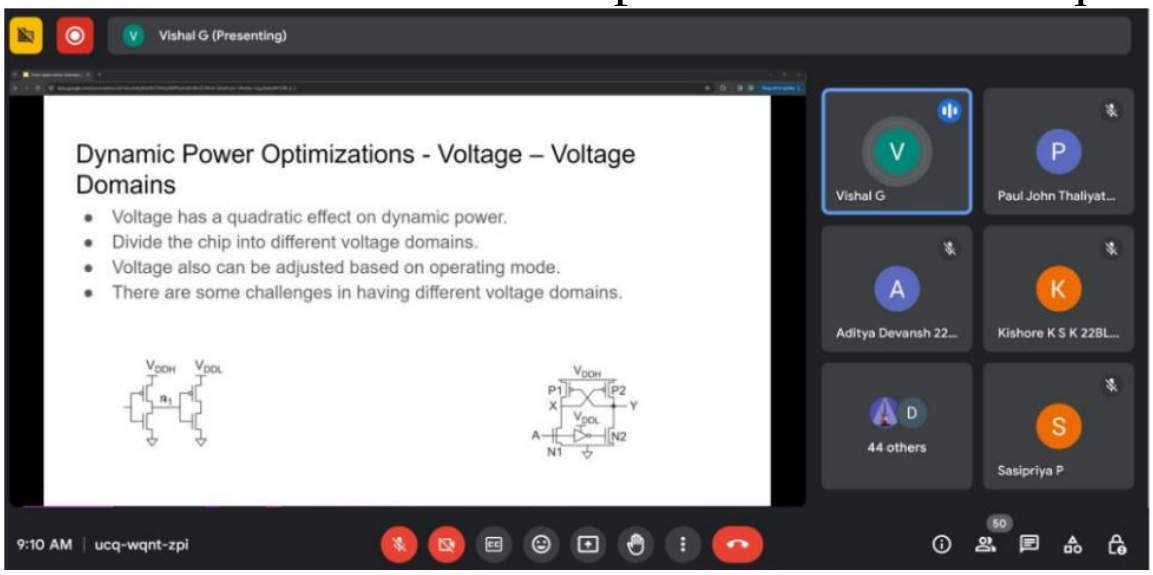
Principal Investigators	**Name of the Agency**	**Title of the Project**	**Total Amount**	**Period of support**	**Completed/Ongoing**
Dr Ananiah Durai. S	VIT Seed Fund	Design and development of hybrid crypto system for secured access of health record	Rs. 3.05 Lakhs	January 2023 to January 2025	Ongoing
PI: Dr Nabihah Ahmad, UTHM University. Co-PI: Dr Ananiah Durai. S	FRGS Grant - Ministry of Higher Education, Malaysia	Duplex AESHA3 Lightweight Crypto-Hardware for Medical IOT Device security with new SubBytes architecture	Rs. 18 Lakhs	01/09/2022 till 31/08/2025	Ongoing
Dr A Prathiba Dr P Augusta Sophy Beulet Dr M Sivagami	VIT SEED FUND	Design and Development of masked PRESENT lightweight block cipher soft IP core	Rs.3.63 Lakhs	till DEC 2024	Ongoing

Workshop on Photonic IC and Microelectronics Design

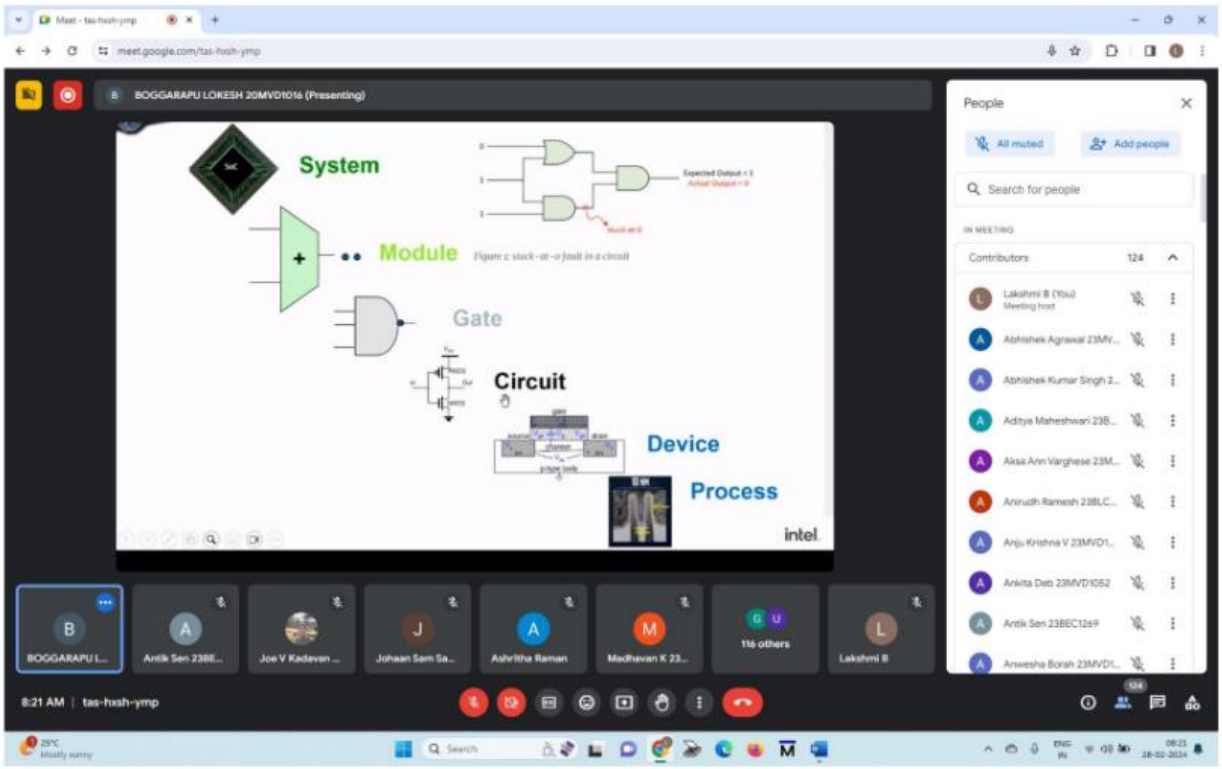




Guest Lecture on Power Optimization Techniques

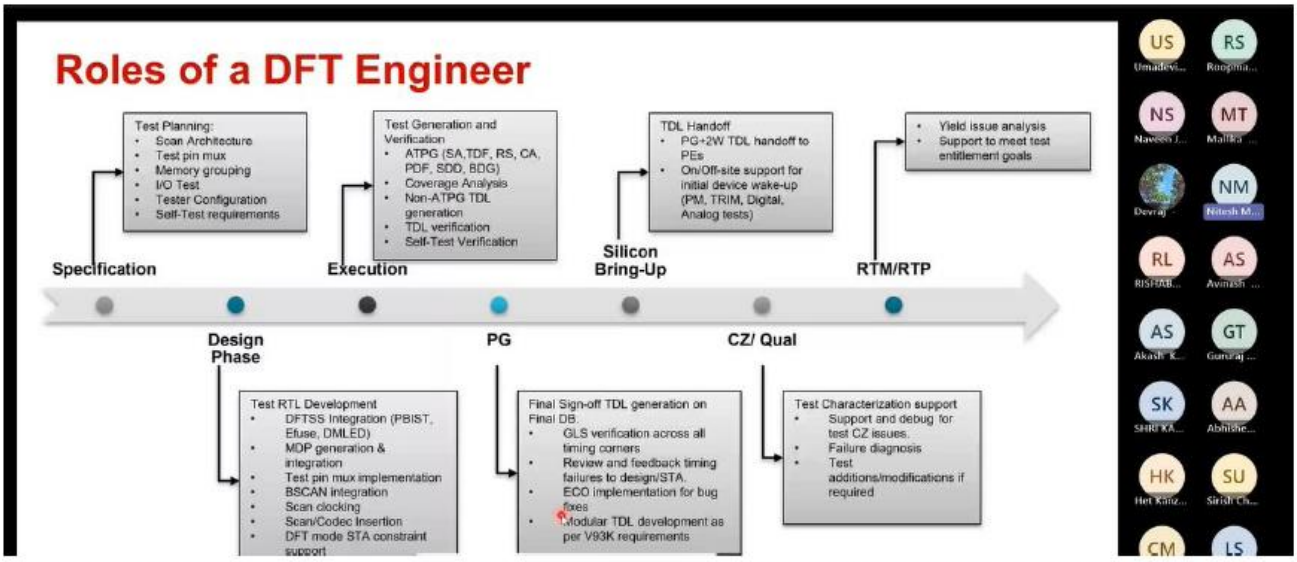


Guest Lecture on VLSI & TCAD: An overview of device, circuit and systems



Guest Lecture on FPGA & ASIC Approaches for Advanced Digital System Design

Guest Lecture on VLSI Testing and Testability



Resource Person Mr. Nitesh Mishra explaining the role of a DFT engineer in an industry to the students